record, neither teaches nor suggests the invention as recited in the claims as presented h rein.

In the invention, a memory cell including a trench having a depth approximating that of the isolation trenches is used to provide a trench capacitor and an isolation trench. Support for Applicants' amendment can be found, for example, in paragraphs [0036], [0047] and [0050]. The memory cell is formed "in a region of the semiconductor substrate in which said plurality of isolation filled trenches are absent." The trench provides electrical isolation of the memory cell from an adjacent memory cell without the need for separate isolation filled trenches. Thus, the invention combines the functions of storage capacitor and electrical isolation into one structure resulting in a reduction in total memory cell area.

In the '697 reference, the memory cell includes two discrete structures, the capacitor trench 14 and the isolation trenches 10, for providing a capacitor for the memory cell and isolation of the memory cell from an adjacent memory cell. The isolation trenches 10 are formed as part of the memory cell and is a discrete structure from the capacitor trench 14. As such, the '697 reference utilizes isolation trenches in close proximity to the capacitor trenches to provide cell-to-cell isolation resulting in an increase in total memory cell area. In the invention, the capacitor trenches also provide cell-to-cell isolation. This is neither shown nor suggested by the '697 reference. If anything, the '697 reference teaches away from the combination of features recited in claim 1. Accordingly, Applicants respectfully submit that the rejection of claims 1-5 and 7 as being anticipated by the '697 reference has been traversed.

In the Office Action, claims 6 and 9 stand rejected under 35 U.S.C. 103 in view of a combination of the teachings of the '697 patent and U.S. patent 5,183,774 ("Satoh"), and claims 8 and 10 stand rejected under 35 U.S.C. 103 in view of a combination of the teachings of the '697 patent and U.S. patent 6.437,369 ("Tang"). In response, Applicants respectfully submit that the Satoh or Tang reference, taken alone or in combination with any other reference of record, neither teaches nor suggests the invention as recited in these claims. As discussed above, Applicants

respectfully submit that the '697 patent does not teach or suggest a trench for providing both a capacitor and isolation for a memory cell. Nowhere in any of these references is there a suggestion of the integrated combination as recited in the subject claims. Accordingly, Applicants respectfully submit that the rejection of record to claims 6 and 8-10 has been traversed.

Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned agent at the telephone number and/or email address set forth below.

Respectfully submitted,

For: Brown et al.

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Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned agent at the telephone number and/or email address set forth below.

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Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claim 1 as follows:

1. (Twice Amended) A structure formed on a semiconductor substrate comprising:
a plurality of isolation filled trenches in the substrate;
a memory cell including a plurality of holes in the substrate, each having a plurality of sidewalls and a bottom wall, said memory cell located in a region of the semiconductor substrate in which said plurality of isolation filled trenches are absent, said holes having a depth proximate that of said plurality of isolation filled trenches;
insulating material present in each of said plurality of holes on said plurality of sidewalls and bottom wall; and
a conductor overfilling each of said holes and extending onto an adjacent upper surface of the substrate;
wherein said plurality of holes electrically isolate said memory cell from an adjacent memory cell.

Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claim 1 as follows:

1. (Twice Amended) A structure formed on a semiconductor substrate comprising:
a plurality of isolation filled trenches in the substrate;
a memory cell including a plurality of holes in the substrate, each having a plurality of sidewalls and a bottom wall, said memory cell located in a region of the semiconductor substrate in which said plurality of isolation filled trenches are absent, said holes having a depth proximate that of said plurality of isolation filled trenches;
insulating material present in each of said plurality of holes on said plurality of sidewalls and bottom wall; and
a conductor overfilling each of said holes and extending onto an adjacent upper surface of the substrate;
wherein said plurality of holes electrically isolate said memory cell from an adjacent memory cell.